Abstract of the Disclosure:

A circuit configuration regenerates clock signals. The circuit configuration includes an input differential amplifier, first and second inverters, and an offset compensation circuit. The input differential amplifier generates first and second amplified signals in response to first and second differential input clock signals. The first and second inverters generate a first and a second differential output clock signal. The offset compensation circuit controls the difference between the two output clock signals to zero or to a constant value. As an alternative to or in supplementation of the offset compensation circuit, it is possible to provide a control circuit for driving the two inverters, which shifts the input pulse shapes of the inverters to the optimum switching point of the inverters. The circuit configuration enables a regeneration of clock signals with simultaneous equalization of pulse distortions.

LDP/nt